IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ken G. Pomaranski et al.	Examiner: Bryan Bui
Serial No.:	10/727,440	Group Art Unit: 2863
Filed:	Dec. 4, 2003	Docket: 200209695-1
Title:	SYSTEM AND METHOD FOR TESTING AN INTERCONNECT IN A COMPUTER SYSTEM	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R § 1.131

Sir/Madam:

We, Ken G. Pomaranski, Andrew H. Barr, and Dale J. Shidla, declare as follows:

1. We are the named co-inventors of the subject matter described and claimed in the above-identified U.S. Patent Application Serial No. 10/727,440, filed December 4, 2003.

2. We have read and understood the Office Action mailed on March 15, 2005 along with the references cited therein and make this Declaration in support of the patentability of the claims of U.S. Patent Application Serial No. 10/727,440, filed December 4, 2003 (the Present Application).

3. I, Ken G. Pomaranski, am a Master Engineer at Hewlett-Packard Company. I began my employment at Hewlett-Packard Company on or about 1989.

4. I, Andrew H. Barr, am a Master Engineer at Hewlett-Packard Company. I began my employment at Hewlett-Packard Company on or about 1995.

5. I, Dale J. Shidla, am an Expert Engineer at Hewlett-Packard Company. I began my employment at Hewlett-Packard Company on or about 1989.

6. This Declaration under 37 C.F.R. § 1.131 is made in response to the rejection of claims 1-9, 11, and 13-19 under 35 U.S.C. §102(e) based on Nejedlo et al., U.S. Patent Application Publication US 2004/0117709 A1 (hereinafter referred to as "Nejedlo"), filed December 16, 2002, and published June 17, 2004.

7. This Declaration under 37 C.F.R. § 1.131 is also made in response to the rejection of claim 1 under 35 U.S.C. §102(e) based on Ellis et al., U.S. Patent Application Publication US 20040117708 A1 (hereafter referred to as "Ellis"), filed March 31, 2003, and published June 17, 2004.

8. This Declaration under 37 C.F.R. § 1.131 is further made in response to the rejection of claims 13 and 17 under 35 U.S.C. §103(a) based on Ellis in view of Nejedlo.

9. Prior to December 16, 2002, the date of filing of Nejedlo, cited by the Examiner as referenced above, and prior to March 31, 2003, the date of filing of Ellis, cited by the Examiner as referenced above, we actually conceived, in the United States, the above-identified and claimed invention of the Present Application. As factual evidence of our conception prior to December 16, 2002, attached hereto and incorporated by reference herein, is Exhibit A.

10. Exhibit A is a confidential internal Invention Disclosure document of Hewlett-Packard Company dated October 22, 2002. This Invention Disclosure document is entitled "METHOD FOR EVALUATING INTERCONNECT QUALITY DURING NORMAL SYSTEM OPERATION" and has an internal Hewlett-Packard Company docket number of HPDN 200209695-1, and was produced prior to the earliest prior art date of December 16, 2002 of Nejedlo and the earliest prior art date of March 31, 2003 of Ellis. This document describes the subject matter of the present patent application and supports that the claimed invention of the present patent application was conceived prior to December 16, 2002.

11. We were diligent in reducing the invention claimed in the Present Application to practice until the invention was brought to the attention of the United States Patent Office on December 4, 2003, with the filing of the Present Application. As factual evidence of our diligence, attached hereto and incorporated by reference herein are Exhibits B and C.

12. Exhibit B is a letter from Hewlett-Packard Company to Patrick G. Billig of Dicke Billig & Czaja PA and is dated April 10, 2003. This document describes the subject matter of the Present Application and was provided to Patrick G. Billig, a patent attorney working on behalf of Hewlett-Packard Company, to draft the Present Application which was later filed on December 4, 2003. This document shows diligence in reducing the invention described in Exhibit A to practice. This document also shows diligence in bringing this invention to the attention of the United States Patent Office.

13. Exhibit C is an e-mail from Christopher P. Kosh of Dicke Billig & Czaja PA, a patent attorney working on behalf of Hewlett-Packard Company, to co-inventors Ken G. Pomaranski, Andrew H. Barr, and Dale J. Shidla dated September 19, 2003 which provided a first draft of the Present Application to each of the inventors for review. The Present

Application was later filed on December 4, 2003. This document shows diligence in reducing the invention described in Exhibit A to practice. This document also shows diligence in bringing this invention to the attention of the United States Patent Office.

14. It is therefore respectfully submitted that the Present Application claims an invention which we conceived prior to December 16, 2002, and we were diligent in reducing the invention to practice prior to December 16, 2002 and up to the constructive reduction of practice of the invention occurring with the filing of the Present Application on December 4, 2003. Thus, the Nejedlo et al. U.S. Patent Application Publication US 2004/0117709 A1 and the Ellis et al. U.S. Patent Application Publication US 20040117708 A1 should be removed as references under 35 U.S.C. § 102(e).

15. We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or patent issued thereon.

Ken G. Pomaranski — Date: 6/13/2005

Andrew H. Barr — Date: 6/13/2005

Dale J. Shidla — Date: 6/13/2005

HPSL

Enter PD Number

Tag Number: T0003573

INVENTION DISCLOSURE

PDNO: 200209695 ATTORNEY: LPG

*Instructions: The information contained in this document is **HP CONFIDENTIAL** and may not be disclosed to others without prior authorization. Submit this disclosure to the HP Legal Department as soon as possible. No patent protection is possible until a patent application is authorized, prepared, and submitted to the Government.*

Red text indicates a required field.

Descriptive Title of Invention:
Method for evaluating interconnect quality during normal system operation

Name of Project:

Product Name or Number:

Submitter Location (City): Roseville California

Was a description of the invention published, or are you planning to publish? If so, the date(s) and publication(s):

No

Was a product or prototype including the invention (i) announced, offered for sale, or sold to any third party (for example, customer, supplier, contract manufacturer), or (ii) sold to HP by, for example, a supplier or contract manufacturer, or (iii) is such activity proposed? If so, when and to whom?:

No

Was the invention disclosed to anyone outside of HP, or will such disclosure occur? If so, the date(s) and name(s):

No

If any of the above situations will occur within 3 months, call your IP Attorney or the Legal Department now at 1-898-4919 or 970-898-4919

Was the invention described in a lab book or other record? If so, please identify (lab book #, etc.)

No

Was the invention built or tested? If so, the date:

No

Was this invention made under a government contract? If so, the agency and contract number:

No

Description of Invention: Please describe your invention in detail using the following outline.

A. Prior solutions and their disadvantages (attach copies of any pertinent product literature, technical articles, patents, etc.).
B. Problems solved by the invention.
C. Advantages of the invention over what has been done before.
D. Description of the construction and operation of the invention.
(include appropriate schematic, block & timing diagrams, drawings, samples, graphs, flowcharts, computer listings, etc.).

Electronic Attachment

List any pertinent patents material to the invention.

List any articles or references or devices pertinent to the invention.

Identify Inventor(s): Pursuant to my (our) employment agreement, I (we) submit this disclosure on this date: 10/22/2002

Employee No. 376567	Name: Ken Gary Pomaranski	Telnet: 748-2436	Mailstop: 5596	Entity & Lab Name: 5260-6815
Employee No. 461531	Name: Andy Harvey Barr	Telnet: 748-2392	Mailstop: 5596	Entity & Lab Name: 5260-6500
Employee No. 345259	Name: Dale John	Telnet: 748-2394	Mailstop: 5596	Entity & Lab Name:

	Shidla			5260-6500
Identify Witness(es): *(It's best to identify the person(s) to whom invention was first disclosed.)*				
The invention was first explained to, and understood by, the witness(es) on this date: 10/22/02				
Name: Robert Dobbs	Employee No. 91866	Telnet: 748-2428	Mailstop: 5596	Entity: 5260-6500
Name:	Employee No.	Telnet:	Mailstop:	Entity:

Inventor & Home Address Information:		
First Inventor's Full Name:		Citizenship:
Street		
City	State	Zip
Do you have a Residential P.O. Address?	Description	
Second Inventor's Full Name:		Citizenship:
Street		
City	State	Zip
Do you have a Residential P.O. Address?	Description	
Third Inventor's Full Name:		Citizenship:
Street		
City	State	Zip
Do you have a Residential P.O. Address?	Description	

Hardcopy Files:

☒ P6 - Method for evaluating interconnect quality during normal system operation.doc

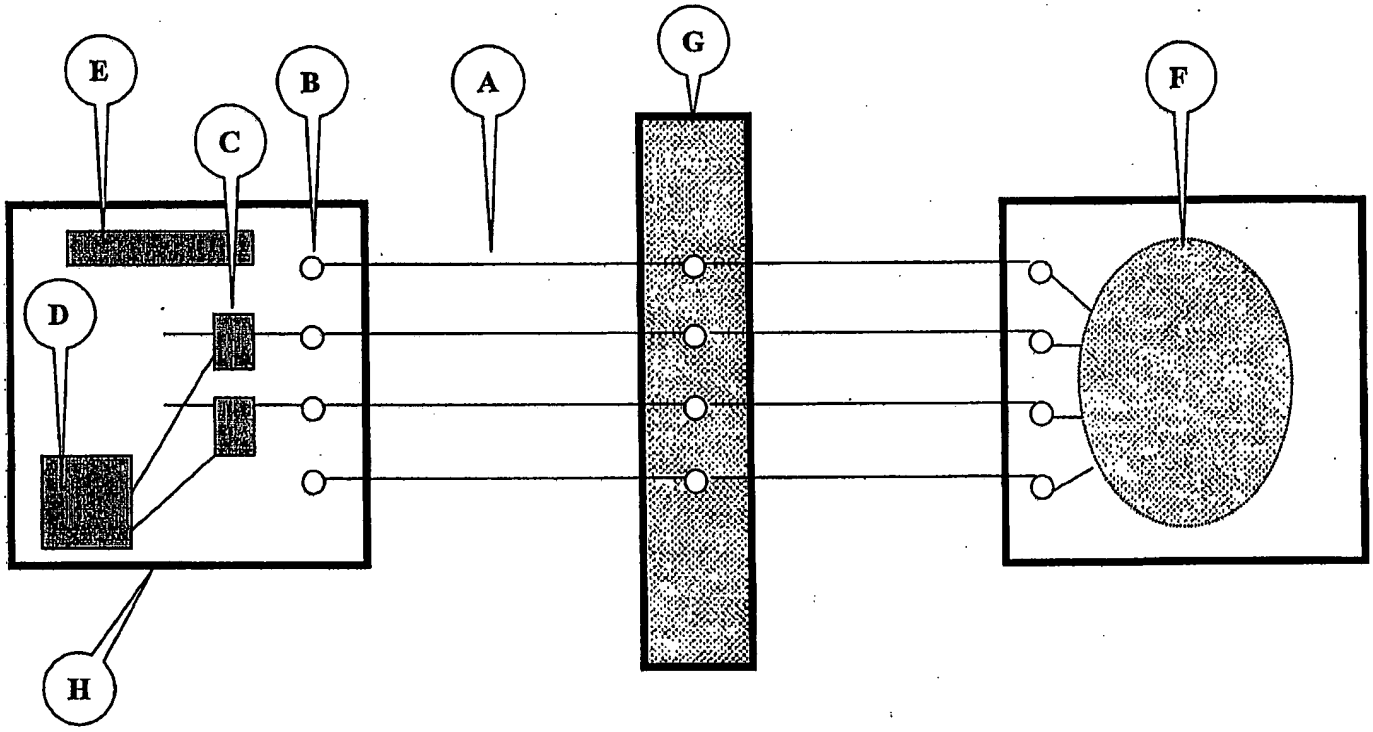
Method for Evaluating Interconnect Quality During Normal System Operation.
10/20/02
Description of the Invention

A. Problem solved by the invention: Interconnect failures in busses present significant challenges to the design and manufacture of high quality systems. In many cases, these failure modes can be predicted by running worst case data patterns through the interface, then evaluating the results. Unfortunately, the typical traffic that traverses an interconnect during normal system operation (while an operating system is running) is not sufficient to predict failures. This invention addresses this problem by allowing for the ability to run worst case data patterns on an interconnect without shutting down the machine, therefore increasing system uptime.
B. Previous solutions and their disadvantages: The current solution to this problem is to perform worst case pattern testing of interface busses during system boot by using boot ROM based self-test. The limitation of this approach is that these tests cannot be performed when the system is up and running an OS. If a bus interface degrades over time (which is a typical failure mode of many interconnects, especially surface mount based sockets and connector systems), it in many cases cannot be detected.
C. Advantages over what has been done before: The method described in this disclosure is superior to current solutions because it provides a means to perform pattern based bus testing without bringing the machine down. This results in higher system availability in two ways:
    1) No reboot needed to test interfaces
    2) Failures can be predicted and dealt with pro-actively before a system crash occurs due to a low quality interconnect.
D. Description of the construction and operation of the invention: The invention consists of the hardware and software algorithms required to perform pattern based testing of bus interfaces during normal system operation.

Figure 1 below shows a block diagram of the hardware implementation of the invention.

Description of FIG 1:
A: Interface bus. Depicted in this diagram as a connection from an ASIC through a connector to another ASIC.
B: ASIC pin that drives the interface bus. Only 4 pins are show in this diagram. Every pin on the interface bus is connected to circuit 'C' as discussed below
C: MUX. Muxes inputs from the normal I/Os of the chip and the state machine (D). The output is chosen by the state machine (D).
D: state machine. Generates bus transactions which are representative of the worst case data patterns. The state machine is set into motion programmatically.
E: Chip error log. This is read by software to determine if any bus errors have occurred (and where on they bus they are occurring).
F: This chip also has interfaces (B,C,D,E). These are represented as the 'oval' for this chip
G: connector.
H: ASIC (which may be socketed).

FIG 1



System level Algorithms required to use the hardware as depicted above. Assume that the bus interface of a CPU chip is being analyzed for potential failures:

1. The CPU chip and it's port on an agent chip is de-allocated from the Operating system by the diagnostic subsystem. This occurs at some appropriate configurable frequency. (once per month, for example).
    a. A spare CPU chip can be logically 'swapped-in' by the diagnostic subsystem if there is a desire to keep the number of CPUs constant during the 'bus check'
    b. GOTO 2
2. The diagnostic subsystem now has control of the CPU. It then performs the following actions:
    a. Read, store and clear chip error logs
    b. Start chip state machines (programmatically)
    c. After pattern test finishes (diags polls state machine status, or waits an appropriate amount of time.) chip error logs are read. If errors are found not found, continue to step 3
    d. # errors found # report errors, keep CPU de-allocated. EXIT ROUTINE
3. report that a 'bus check' has been performed..
4. return CPU to the available pool of system resources

EXHIBIT B

Hewlett-Packard Company
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April 10, 2003

Patrick G Billig
Dicke Billig & Czaja PA
Fifth Street Towers
100 South Fifth Street
Suite 2250
Minneapolis, MN 55402

RE: Preparation of Patent Application
Pursuant to Outside Counsel Procedures Dated November 2001
HP Reference No.:200209695-1
Entitled: Method For Evaluating Interconnect Quality During Normal System Operation
HP Required Date: Aug. 10, 2003

Dear Patrick:

We would like you to provide a quote of the cost for your firm to prepare a US Patent application based on the HP Invention Disclosure identified above, a copy of which is enclosed.

Your quote should be based on preparing an application including the items noted on the enclosed Outside Counsel Checklist and according to HP's Outside Counsel Procedures referenced above, for filing by our Required Date.

Your quote should be submitted on the enclosed Request for Quote and Engagement Letter Agreement. If your quote is accepted, we will return a fully executed copy of the Agreement to you for your records. **The Agreement will not be binding on you or on HP until signed by HP's authorized representative.**

If the Agreement is not signed and returned to HP, any bills submitted by you cannot be paid.

Thank you for your assistance in reviewing this invention disclosure. If your review indicates a possible conflict for your firm, you should advise us within one week of receipt of this letter.

Sincerely,

Sent via email by Jerry Dechant for David Plettner

David A Plettner

Enc.: HP Invention Disclosure
RFQ
Filing Procedures Checklist

From: Christopher Kosh
To: andrew.barr@hp.com; dale.shidla@hp.com; ken.pomaranski@hp.com
Date: 9/19/03 10:42AM
Subject: Patent application 1st draft for invention disclosure 200309695-1 (Our ref. 300.221.101)

Dale, Andrew, and Ken,

Please find the attached patent application draft and figures for invention disclosure 200309695-1 for your review and comment.

The attached files are password protected. The password is the same password used for the draft for 200308580-1.

We look forward to receiving your comments.

Regards,

Chris

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CC: Billig, Patrick; Dauphinais, Denyse; Elseth, Kathryn